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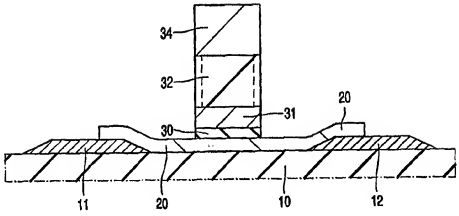

(57) Abstract

In an insulated-gate top–gate thin film transistor, the insulated gate structure comprises a first gate insulator layer over the semiconductor body of the transistor, an intermediate conductive layer over the first gate insulator layer, a second gate insulator layer over the intermediate conductive layer and a gate conductor over the second gate insulating layer. The intermediate conductive layer enables the two insulator layers to be etched under separate conditions, and also acts as a field plate to reduce the effect of negative undercut in the top insulator layer.

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Thin film transistors and their manufacture.

DESCRIPTION

This invention relates to thin film transistors (hereinafter termed TFTs) and their manufacture, and particularly to top-gate TFTs. TFTs are commonly employed in flat panel displays (for example, an active-matrix liquid-crystal display) and in other types of large-area electronic devices. The invention also relates to such devices.

There is much interest in developing arrays of TFTs which may form the switching elements in a cell matrix, for example in a flat panel display as described in United States Patent US-A-5,130,829, the whole contents of which are hereby incorporated herein as referenced material. The TFT devices may be fabricated with portions of an amorphous or polycrystalline semiconductor film to form the body of the transistor devices.

One advantage of a top-gate TFT structure, compared to a bottom-gate TFT, is the ease with which a low resistance gate line can be made with a highly conductive top-gate metal such as aluminium.

It is known to provide a two-layer gate insulating structure. This enables the lower layer to be deposited over the silicon layer before the silicon layer is patterned to define the silicon regions of the individual TFTs. By depositing the lower gate insulator layer over the semiconductor layer before any patterning of the semiconductor layer, the electrical properties of the interface between the semiconductor layer and the lower gate insulator layer are improved. The lower gate insulator and the semiconductor layer are etched together to define the semiconductor island of each transistor, and the upper gate insulating layer is deposited over this structure.

One difficulty in the manufacture of a top gate TFT is the production of a vertical profile in the gate dielectric, which is aligned with the metal gate,

using a process that does not etch away the underlying semiconductor layer. This difficulty arises because the top gate insulator layer is required to have a sufficient thickness to provide insulation between the gate conductor and the source conductor at the positions over the substrate where these two conductors overlap. However, as the thickness of the gate insulator increases, the difficulty of avoiding damage to the underlying silicon layer during etching also increases.

According to the present invention there is provided an insulated-gate top-gate thin film transistor wherein the insulated gate structure comprises a first gate insulator layer over the semiconductor body of the transistor, an intermediate conductive layer over the first gate insulator layer, a second gate insulator layer over the intermediate conductive layer and a gate conductor over the second gate insulating layer, the second gate insulator layer being thicker than the first gate insulator layer.

The intermediate conductive layer, which forms part of the gate insulating structure, can act as an etch stop layer to enable the top, second gate insulator layer to be etched under the optimum conditions for producing a vertical profile aligned with the gate conductor, without having to compromise by using etching conditions which do not attack the underlying semiconductor layer.

The lower, first gate insulator layer is then only a relatively thin layer, which allows etching to be performed for a much shorter time with less risk of damage to the underlying semiconductor layer.

The intermediate conductive layer also acts as a field plate at a uniform potential, so that satisfactory operation of the transistor is ensured provided there is correct alignment of the field plate. The exact profile of the thicker second gate insulator layer is therefore less critical than in known processes.

The first gate insulator layer may have a thickness of between 40 and 80 nm. The semiconductor layer may have a thickness of approximately 40 nm, so that the lower insulator layer has a comparable thickness to that of the

semiconductor layer. The thicker, second gate insulator layer may have a thickness of between 200 and 300 nm, and thereby provides insulation at cross-over points of the upper gate electrodes and the lower source or drain electrodes of the transistor.

Both gate insulator layers preferably comprise silicon nitride, and the first gate insulator layer may preferably comprise silicon-rich silicon nitride. This may improve the on conductance of the TFT.

The transistor is preferably an amorphous silicon TFT.

The invention also provides an electronic device comprising an array of thin film transistors of the invention, and the device may, for example, comprise a liquid-crystal display.

The invention also provides a method of manufacturing a thin film transistor having an insulated gate structure provided over a semiconductor layer which defines the body of the transistor and which is arranged as a semiconductor island, the insulated gate structure being formed by:

depositing a first insulator layer, an intermediate conductor layer and a second insulator layer over the semiconductor layer;

depositing and patterning a gate conductor layer over the second insulator layer;

patterning the second insulator layer by etching to the intermediate conductor layer; and

patterning the intermediate conductor layer and the first insulator layer by etching to the semiconductor layer.

According to the method of the invention, the two gate insulator layers are etched by separate etching processes, so that these processes may be optimised for the individual layers. Thus, for the thicker upper, second insulator layer etching is carried out to the intermediate conductor layer so that no account needs to be taken of the underlying silicon layer in the selection of the etching process for the upper insulator layer.

The method preferably initially comprises the steps of:

depositing and patterning a metallic layer over an insulating substrate to define source and drain electrodes; and

depositing the semiconductor layer over the patterned metallic layer.

This provides a top gate staggered TFT structure. The first insulator layer and the semiconductor layer may both be patterned to define the semiconductor island before the deposition of the intermediate conductor layer. This enables the optimum conditions to be maintained for the interface between the semiconductor layer and the adjacent first insulator layer.

Embodiments of the invention will now be described by way of example with reference to the accompanying drawings in which:

Figure 1 shows in plan view a pixel of a display device incorporating a thin film transistor of the invention;

Figure 2 is a cross sectional view of a thin film transistor at stages in its manufacture by a known method;

Figure 3 illustrates undercut problems which can result during the method illustrated in Figure 2; and

Figure 4 is a cross sectional view of a TFT at stages in its manufacture by a method in accordance with the invention.

It should be noted that these Figures are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings.

Top-gate TFTs according to the invention, and manufactured in accordance with the invention may form the switching elements of a display matrix or other large area electronic device, for example, as disclosed in US-A-5,300,449. By way of example, Figure 1 shows the whole area of one cell of an active switching matrix of a flat panel display manufactured in accordance with the invention. A cell comprises an electrode pattern 11 and 12 of, for example, ITO formed on an insulating substrate 10. The substrate

10 may comprise a back plate of the display, for example a glass plate or polymer film. Column conductors 11 of the pattern 11, 12 form common source lines of the switching TFTs in the matrix columns. Another part 12a of the pattern 11, 12 forms a drain electrode of the TFT. In this particular exemplary embodiment, the bulk of Part 12 of the pattern 11,12 forms a pixel electrode 12b. This pixel electrode 12b is integral with the drain electrode part 12a and also, in this example, with a part 12c which forms the bottom electrode of a pixel storage-capacitor with a row conductor 25 of a neighbouring cell. The row conductors 25 form common gate lines of the TFTs in the matrix rows. The switching TFT of each cell comprises a silicon transistor body 20a. In the example of Figure 1, these bodies 20a are in the form of separate islands of a silicon film pattern. Typically, the silicon film 20 is of, for example, a-Si:H. However, rather than amorphous silicon, polycrystalline silicon may be preferred for some displays and/or other large-area electronic devices.

Figure 2 illustrates some steps in a known manufacturing process for producing thin film transistors suitable for use in the device described with reference to Figure 1. For the purposes of explanation, the cross sectional views in Figure 2 are taken along the line X-X in Figure 1.

The process comprises the steps of forming a source and drain electrode pattern 11, 12 on a substrate 10. For example, an ITO conductor layer may be deposited on a glass substrate 10, and wet etching may be performed in order to define the source and drain electrode pattern. A silicon film 20 is deposited on the source and drain electrode pattern 11, 12 to provide the transistor body 20a comprising the channel area 20c of the TFT. A first gate insulator layer 30 is provided over the semiconductor layer 20, and the first gate insulator layer 30 and the semiconductor layer 20 are patterned using the same mask to define the semiconductor island forming the transistor body 20a. This results in the structure illustrated in Figure 2 Part A. The deposition of the first gate insulator layer 30 over the semiconductor layer 20 before patterning of the semiconductor 20 improves the electrical

characteristics of the interface between the insulator layer 30 and the semiconductor layer 20.

A second, upper gate insulating layer 32 is then deposited over the array and a gate conductor 34 is provided over the upper gate insulator 32.

The two gate insulator layers and the gate conductor layer 34 are patterned together using a common photolithographic mask on the gate conductor 34.

The source and drain regions 20s and 20d may be doped, for example using plasma doping with the top gate structure 30, 32, 34 masking the underlying intrinsic semiconductor channel area 20c. Alternatively the source and drain regions 20s, 20d of the semiconductor layer 20 may be formed by ion implantation, using the top-gate structure as an implantation mask.

The steps illustrated in Figure 2 are described in greater detail in International Patent Application IB 97/01529 published as WO 98/27583 (Our ref: PHB 34127), which additionally describes the implementation of source and drain silicide parts overlying the source and drain regions 20s, 20d of the semiconductor layer 20. IB 97/01529 is incorporated herein as reference material.

One problem with the process described with reference to Figure 2 is the difficulty in obtaining vertical side walls for the insulated gate structure (such as shown schematically in Figure 2). The combined thickness of the two gate insulating layers 30, 32 with respect to the thickness of the semiconductor layer 20 requires the etching process to be controlled very precisely in order to prevent attack by the etchant of the semiconductor layer 20. Furthermore, since the etchant for removing the gate insulator layers 30, 32 must be selected to have the least possible effect on the semiconductor layer, the etching conditions can not be optimised solely with respect to the insulator layers. It is therefore difficult to prevent negative or positive undercuts during the etching of the gate insulator layers.

Figure 3 part A illustrates schematically the effect of negative undercut during the etching of the gate insulator. When doped source and drain

regions 20s, 20d are to be implemented, for example using the gate conductor as an ion implantation mask, the effect is that the top gate shadows some of the underlying silicon from the implantation, so that undoped regions 201 remain adjacent the channel, increasing the series resistance of the TFT.

Figure 3 part B illustrates schematically the effect of positive undercut during the etching of the gate insulator. The effect is that part of the channel 20b beneath the gate is not modulated by the gate. This part of the channel is not doped and therefore the increased series resistance again results.

Figure 4 illustrates a method in accordance with the invention, for the manufacture of a thin film transistor of the invention.

Figure 4 Part A corresponds to Figure 2 Part A, so that known photolithographic and etching techniques have been employed to form the electrode pattern 11, 12 from a film of electrode material deposited on the insulating substrate 10. The electrode material may, for example, comprise ITO. The semiconductor layer 20 is an undoped silicon film, and preferably comprises hydrogenated amorphous silicon, and the lower, first gate insulating layer 30 may for example comprise silicon nitride.

In the case of amorphous silicon, the silicon layer 20 may have a thickness of approximately 40 nm, and the lower gate insulator layer 30 preferably has a thickness of between 40 and 80 nm. The silicon nitride layer 30 may comprise silicon-rich silicon nitride, which has been found to reduce the interface state density at the insulator/semiconductor boundary. A two-layer gate insulator 4 for an insulated-gate TFT structure is described in the article "Amorphous Silicon Thin Film Transistors with Two-layer Gate Insulator" from Appl. Phys. Lett. 54 (21), 22 May 1989, pages 2079 to 2081.

In accordance with the invention, an additional conducting layer 31 is deposited over the array as shown in Figure 4 Part B, and using known techniques. This conductive layer 31 may comprise a metal layer, for example aluminium, or may comprise a semiconductor layer which is preferably subsequently doped to increase the conductivity.

The upper, second gate insulator layer 32 and the gate electrode layer

34 are then deposited, in the manner described with reference to Figure 2 Part B.

The gate electrode layer 34, for example aluminium, is etched in a conventional manner using an appropriate etchant and a photolithographic mask. For example, the metal gate may be wet etched. The upper, second gate insulator layer 32 is then etched using the same photolithographic mask, and using an etchant for which the conductive layer 31 acts as an etch stop. A dry, reactive ion etching process may be employed for this purpose, which can be controlled to provide vertical side walls for the insulator layer 32.

Using the same photolithographic mask, the conductor layer 31 is etched, and the lower insulator layer 30 may then be removed using a wet etching process. This wet etching process should produce a minimum undercut because the thickness of the lower gate insulator 30 can be kept to a minimum. The gate conductor layer 34 may itself be used as a mask for the etching of the insulator layers 30 and 32.

The conducting layer 31 acts as a field plate in the TFT structure, so that if the upper, first gate insulator layer 32 is over etched (for example as shown in dotted lines in Figure 4 Part C) or if there is some undercut, the field plate defined by the conductor layer 31 provides a uniform potential layer which redistributes the electric field over the entire width of the channel.

A silicide-forming metal (for example chromium) may also be deposited to enable silicide areas to be formed over the source and drain areas of the TFT structure, to reduce the contact resistance at the source and drain of the TFT. This process is described in International Patent Application IB 97/01529.

As described above with reference to Figure 2, the TFT may also have doped source and drain regions, which may be formed by plasma doping using the top-gate structure 30, 31, 32, 34 to mask the underlying channel area, or they may be formed by ion implantation, using the top-gate structure 30, 31, 32, 34 as an implantation mask. The doping may alternatively be performed by doping the silicon film 20 from the bottom source and drain

electrode pattern 11, 12, for example as described in European Patent Application EP-A-0 221,361.

The vertical side-walls of the gate structure, and particularly the avoidance of undercuts as shown in Figure 3 is particularly important when ion implanted source and drain regions of the semiconductor layer 20 are to be formed. It is desirable that the ion implanted regions butt against the modulated channel area of the semiconductor layer. The invention enables positive or negative undercut to be substantially avoided, particularly in the gate dielectric layer 30 between the intermediate conductor layer 31 and the silicon layer 20. This enables accurate ion implantation of the source and drain regions 20s, 20d of the silicon layer 20, which assists in limiting series resistances in the TFT structure.

Furthermore, the function of the conductor layer 31 as a field plate ensures that the full channel area is modulated by the gate, thereby avoiding the problems associated with positive undercut as described with reference to Figure 3 part B. If some negative undercut in the upper gate insulator layer cannot be avoided, shadowing as described with reference to Figure 3 part A is also avoided, because the lower gate insulator provides the insulator/channel interface.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design and use of thin-film transistors, circuits and component parts thereof and which may be used instead of or in addition to features already described herein.

CLAIMS

1. An insulated-gate top-gate thin film transistor wherein the insulated gate structure comprises a first gate insulator layer over the semiconductor body of the transistor, an intermediate conductive layer over the first gate insulator layer, a second gate insulator layer over the intermediate conductive layer and a gate conductor over the second gate insulating layer, the second gate insulator layer being thicker than the first gate insulator layer.

2. A thin film transistor as claimed in claim 1, wherein the first gate insulator layer has a thickness of between 40 and 80 nm.

3. A thin film transistor as claimed in claim 1 or 2, wherein the semiconductor layer has a thickness of approximately 40 nm.

4. A thin film transistor as claimed in any preceding claim, wherein the second gate insulator layer has a thickness of between 200 and 300 nm.

5. A thin film transistor as claimed in any preceding claim, wherein both gate insulator layers comprise silicon nitride.

6. A thin film transistor as claimed in claim 5, wherein the first gate insulator layer comprises silicon-rich silicon nitride.

7. A thin film transistor as claimed in any preceding claim, wherein the semiconductor layer comprises amorphous silicon.

8. A thin film transistor as claimed in any preceding claim, wherein the semiconductor body of the transistor comprises doped source and drain

regions.

9. An electronic device comprising an array of thin film transistors as claimed in any preceding claim.

10. An electronic device as claimed in claim 8 comprising a liquid-crystal display.

11. A method of manufacturing a thin film transistor having an insulated gate structure provided over a semiconductor layer which defines the body of the transistor and which is arranged as a semiconductor island, the insulated gate structure being formed by:

depositing a first insulator layer, an intermediate conductor layer and a second insulator layer over the semiconductor layer;

depositing and patterning a gate conductor layer over the second insulator layer;

patterning the second insulator layer by etching to the intermediate conductor layer; and

patterning the intermediate conductor layer and the first insulator layer by etching to the semiconductor layer.

12. A method as claimed in claim 11, initially comprising the steps of:

depositing and patterning a metallic layer over an insulating substrate to define source and drain electrodes; and

depositing the semiconductor layer over the patterned metallic layer.

13. A method as claimed in claim 12, wherein the first insulator layer and the semiconductor layer are both patterned to define the semiconductor island before deposition of the intermediate conductor layer.

14. A method as claimed in any one of claims 11 to 13, wherein the

intermediate conductor layer and the second insulating layer are patterned by separate etching steps.

15. A method as claimed in any one of claims 11 to 14, wherein the second insulator layer, the intermediate conductor layer and the first insulator layer are each patterned to correspond approximately in shape to the patterned gate conductor.

16. A method as claimed in any one of claims 11 to 15, wherein the semiconductor layer comprises amorphous silicon.

17. A method as claimed in any one of claims 11 to 16, further comprising the step of ion implantation into the semiconductor layer to define doped source and drain regions of the thin film transistor.

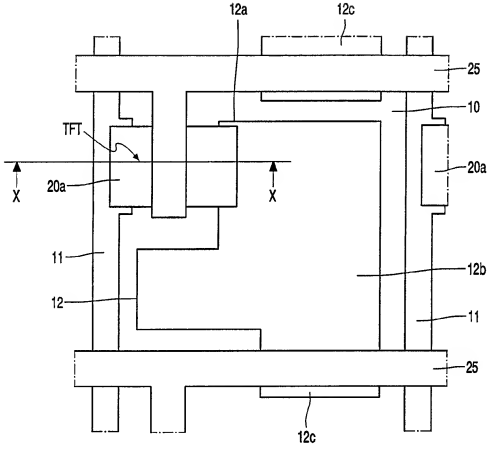

FIG. 1

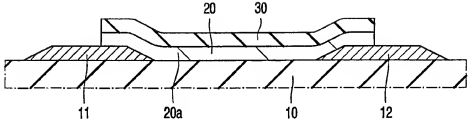

FIG. 2A

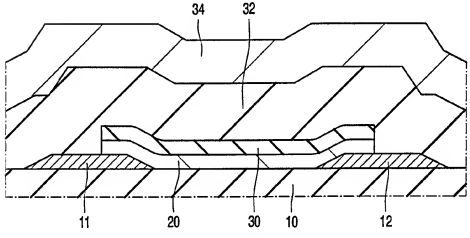

FIG. 2B

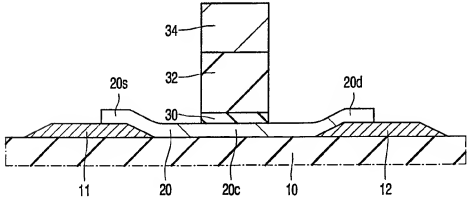

FIG. 2C

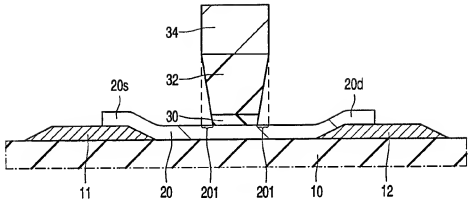

FIG. 3A

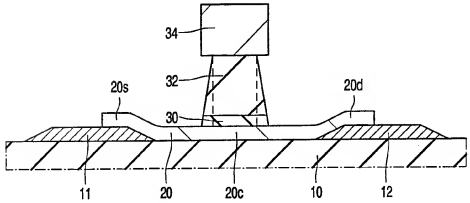

FIG. 3B

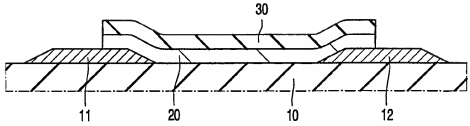

FIG. 4A

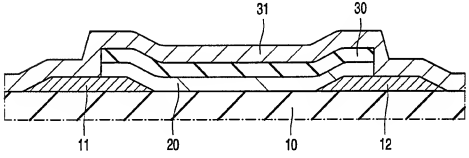

FIG. 4B

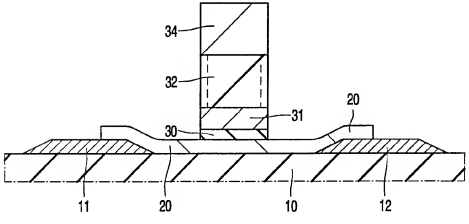

FIG. 4C

INTERNATIONAL SEARCH REPORT

Interr nal Application No
PCT/EP 99/05777

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/336 H01L29/786 H01L29/49

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 751 037 A (AOZASA HIROSHI ET AL) 12 May 1998 (1998-05-12) figures 12,19,21,23 column 16, line 4 - line 15 column 19, line 53 - line 60 column 20, line 62 -column 21, line 4 column 22, line 36 - line 47	1,8,9
A		2-4,11, 13-15,17

X	PATENT ABSTRACTS OF JAPAN vol. 017, no. 418 (E-1408), 4 August 1993 (1993-08-04) -& JP 05 082787 A (SONY CORP), 2 April 1993 (1993-04-02)	1,8,9
A	abstract; figures 1,4	2-7,11, 13-17

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 November 1999	25/11/1999
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Polesello, P

Form PCT/ISA/210 (second sheet) (July 1992)

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PCT/EP 99/05777

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 446 299 A (ACOVIC ALEXANDRE ET AL) 29 August 1995 (1995-08-29) figure 1 column 3, line 36 - line 57 column 4, line 31 - line 54	1,8
A		2-7,11, 13-17

P,X	US 5 929 479 A (OYAMA KENICHI) 27 July 1999 (1999-07-27) figures 1,2,4F,4G,5,6F,6G column 1, line 23 - line 29 column 1, line 61 -column 2, line 8 column 4, line 53 - line 65 column 7, line 31 -column 8, line 11 column 9, line 40 -column 10, line 9	1,7,8
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X	& DATABASE WPI Section EI, Week 199830 Derwent Publications Ltd., London, GB; Class U11, AN 1998-339405 OYAMA K: "Non volatile semiconductor memory with floating gate for multivalue information storage - has second control gate electrode arranged on second floating gate electrode via fourth gate insulating film" & JP 10 125810 A (NEC CORP), 15 May 1998 (1998-05-15)	1,7,8
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A	WO 98 27583 A (PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 25 June 1998 (1998-06-25) cited in the application figures 1-8 page 5, line 13 -page 9, line 3	1-17

A	US 5 008 218 A (MIMURA AKIO ET AL) 16 April 1991 (1991-04-16) figures 2A-2F column 4, line 21 - line 62	1-4, 8-11, 13-15,17

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International Application No
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